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FinFET Based Low Power Techniques for the Power Management of IoT Devices

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Research article

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Abstract

The ability of IoT devices to self-power is a crucial requirement for achieving self-sustainability. The design of such a system requires a notable maintenance cost that emphasizes the demand for developing battery-less IoT devices. This paper presents a novel FinFET-based power management circuitry for an IoT application. Energy management is addressed by coupling low-power features in hardware with low-power system-level techniques. The market demand and surge in portable electronic devices have pushed the semiconductor industry to create circuit designs functioning at Low Voltage (LV) for Low Power (LP) consumption. Leakage power has become a severe problem in LV and LP devices. The superior performance of FinFETs in the subthreshold region makes them a viable substitute for CMOS devices. The application considered in this work is IoT-based wireless lighting and shading control. Indoor solar cells are used to power the IoT-based controller that drives the luminaire and window blinds. This paper applies different leakage reduction techniques, such as forced stacking, sleepy transistor, and Dual VDD methods, to FinFET based and CMOS-based circuits. An analysis of the different power components, static and short circuit power is also carried out using LTSpice.

Keywords: Converters, Energy harvesting, MOS integrated circuits, Lighting control, SPICE, Leakage currents.

1. Introduction

Power management plays a significant role in IoT devices, as they extend their capabilities to include artificial intelligence-based edge processing and self-powered devices. If trillions of IoT devices are powered by batteries that can last approximately 10 years, the number of batteries that need to be replaced each day is 274 million. Powering IoT devices using ambient light sources paves the way for building autonomous IoT systems due to their high efficiency and low cost [1]. Most IoT-based home automation systems require power in the microwatt range provided by indoor photovoltaics.

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Currently, energy harvesting is needed, particularly for biomedical applications such as body-based and wireless sensor networks (WSNs) situated in remote areas and low-power consumer electronics [3]. Investigating alternative energy sources for powering these networks, such as vibration, temperature gradients, radio frequency (RF), and pressure changes, is crucial. The effects of energy harvesting, dynamic voltage, and frequency scaling, and proper clock distribution enhance the lifetime of IoT devices by increasing the amount of available energy while reducing their power consumption. The design of a power converter forms a critical building block for an energy harvesting circuit. A converter aims to increase the DC level of the harvested signal from mV to Volts.

Power converters are essential in energy harvesting systems and portable electronic devices such as cellular phones and laptops [4]. DC/DC converters can supply the different voltage levels required by different subcircuits

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instead of using multiple batteries to achieve that voltage level, thereby saving space. An energy harvesting system must have a DC/DC converter that can increase the very low voltage produced during indoor energy harvesting to a usable output because this voltage is much lower than what is needed for most integrated circuits (ICs) [5, 6].

The field of transistor architecture has evolved over time, from planar to transistor to FinFET technology. Due to quantum tunneling, electrons are more likely to move between the source and drain regions of transistors as they decrease. A rise in leakage current is caused when a source-drain voltage is applied, even in the absence of a gate voltage. The wrap-around structure of FinFET allows for greater control over the leakage current. Therefore, FinFET has become a viable alternative to traditional MOSFET in CMOS-based digital circuit design for low-power applications [7].

FinFETs are promising for use in energy harvesting circuits. To reduce leakage currents, enhance system performance, and provide ultralow voltage operation of an energy harvesting system, DC/DC converters can be fabricated using new technologies such as Silicon–On–Insulator (SOI) FinFETs and CNFETs instead of the standard CMOS process. A multigate MOSFET device formed on a substrate with the gate wrapped around the channel is called a FinFET. The name FinFET comes from the fact that the source-drain region forms on the silicon surface. FinFET devices can have feature sizes as small as 20 nm, 30% faster switching times, and less leakage current [8].

Devices such as FinFETs form the basis for the fabrication of modern nano-electronic semiconductor devices and have become the dominant gate design at 14 nm, 10 nm, and 7 nm process nodes. FET and FinFET devices differ because the FinFET channel (conducting) is encircled by a thin band of silicon called the "fin", which makes up the device body. The fin thickness determines the track's effective length, and the wrapped gate provides the best electrical control over the medium [9]. By doing this, effects of short channels are lessened and the leakage current is reduced [10]. Three modes of operation exist for FinFETs: low power (LP), independent gate (IG), and shorted gate (SG) [11].

The main contributions of this paper include the following:

- Use of indoor energy harvesting for powering IoT-based sensor nodes.
- Design of FinFET-based low-power circuit techniques and analysis of leakage and short-circuit power.
- Use of FinFETs in the power converter design for energy harvesting applications.

2. Literature Review

The power consumption in Very Large-Scale Integration (VLSI) is divided into dynamic and static categories. As a result, dynamic and static power reduction should be considered when designing low-power VLSI circuits [12].

The overall energy per clock cycle of a VLSI system consists of dynamic energy, leakage energy and short- circuit energy (negligible) as shown in (1).

$$E_{overall} = \alpha_L C_L Vdd^2 + Vdd * I_{off} T_{CK} \quad (1)$$

where α is the switching activity, C_L is the load capacitance, Vdd is the supply voltage, I_{off} is the leakage current (OFF current) and T_{CK} is the clock cycle that results from multiplying the number of cascading logic gates by the average gate delay occurring inside the critical path [13].

The first term in (1) corresponds to the dynamic energy E_{dyn} and the second term in (1) corresponds to the leakage energy E_{lkg}. A reduction in Vdd leads to a squared reduction in $E_{dyn}$and an exponential increase in E_{lkg}. A decrease in the supply voltage results in an almost exponential increase in the gate delay, a minor drop in I_{off} because of the Drain Induced

Barrier Lowering (DIBL) effect, and a linear decrease in the first factor (Vdd). Alioto et al., described the trends of leakage and dynamic energy with VDD. It is observed that leakage energy dominates for $V_{dd} < V_{dd,opt}$ (Value of VDD at Minimum Energy Point) and that dynamic energy dominates for $V_{dd} > V_{dd,opt}$ [14].

Even though the short-circuit power is ignored in equation (1) because of its small value, the circuit power dissipation increases as the MOSFET threshold voltage decreases to maintain high-speed operation when the supply voltage is reduced [15].

The static noise margin, write margin, lowest supply voltage needed, and leakage power consumption of FinFET-based SRAM cells were significantly improved in 6T and 8T-SRAM cells [17, 18]. Farkhani et al., [16] compared FinFET-based and CMOS devices in these tests.

Additional circuits utilizing FinFETs include CMOS amplifiers, Schmitt triggers, and an operational transconductance amplifier circuit, which is essential for high-performance, low-noise ICs used in analog applications, as covered in [19].

Various circuit-level technologies, such as subthreshold, multithreshold, and adiabatic circuits [19], have been proposed in the literature to lower dynamic power. Adiabatic logic is a novel low-power circuit structure that recycles circuit energy using an AC supply instead of a DC supply.

The use of a low-power FinFET in adiabatic circuit structure improved the performance. Therefore, leakage suppression and performance improvement also apply to FinFET adiabatic circuit structures [20].

Several harvesters, such as kinetic energy harvesting [21], vibrational energy harvesters [22], photovoltaic energy harvesters [23], and wind energy harvesters [24] are being used to develop self-powered embedded systems.

There are three types of power converters: linear regulators, inductive power converters, and switched capacitor converters. Of these, a switched capacitor-based converter is appropriate for IoT applications due to its high-power density at efficiency equal to that of other regulators and its integration capabilities [25]. A buck converter is a DC/DC converter that produces a DC voltage lower than the input voltage, i.e., Vout < Vs. A boost converter is a DC/DC converter that produces a DC voltage higher than the input voltage, i.e., Vout > Vs. When indoor solar power is insufficient for the load demand need, the battery charge controller can be employed for power correction in voltage-current mode [26].

3. Modeling of FinFET

The short channel effects (SCE), such as the threshold voltage 'Vt' roll-off, DIBL, and hot carrier effects, limit the use of conventional planar MOS transistors. These effects all cause leakage currents such as SL, gate direct tunneling leakage, and hot carrier effects as devices decrease than 50 nm. While lowering the power supply reduces the effects of power and hot carriers, it degrades the circuit's performance. Lowering Vt can improve this performance. However, this results in an increase in subthreshold leakage.

Thus, a double gate device will be needed to continue shrinking. Double gate MOSFETs (DGFET) are MOSFETs with two gates used to control the channel, improving the gate channel control and providing greater resilience to SCE. This increases the physical gate thickness, thereby reducing the leakage currents.

The device width W of the FinFET is given by:

$$W = 2H_{fin} + T_{fin} \quad (2)$$

where H_{fin} is the fin height and T_{fin} is the fin thickness.

The front gate voltage V_{GfS} and back gate voltage V_{GbS} in the case of a fully depleted thin body DGFET were derived in [31,32, 33].

For FinFETs $V_{GfS} = V_{GbS} = V_{GS}$, the expression for V_{GS} becomes,

$$V_{GS} = \psi_{sf} + \frac{1}{1+r}\left[(V_{FBf} + rV_{FBb}) - \left(\frac{Q_{cf}}{C_{of}} + r\frac{Q_{cb}}{C_{ob}}\right) -\right.$$

$$\left(\frac{Q_b}{2C_{of}} + r\frac{Q_b}{2C_{ob}}\right)\Big] \quad (3)$$

where r, termed the gate coupling factor, is given by:

$$r = \frac{C_b C_{ob}}{C_{of}(C_b + C_{ob})} \quad (4)$$

ψ_{sf} is the front surface potential; Q_{cf} is the front surface inversion charge density, and Q_{cb} is the back surface inversion charge density, Q_b is the depletion charge density, C_{of} is the front gate oxide capacitance, C_{ob} is the back gate oxide capacitance and C_b is the depletion capacitance.

The threshold voltage $V_{Tf(asymm)}$ for a thin, fully depleted asymmetric DGFET is given as:

$$V_{Tf(asymm)} = \psi_{sf} + \frac{1}{1+r}\Big[(V_{FBf} + rV_{FBb}) - \left(\frac{Q_b}{C_{of}} - r\frac{Q_b}{2C_b}\right)\Big] \quad (5)$$

Eqs. (2)-(5) are used to study the effect of the front gate and back gate voltages on the threshold voltage of the FinFET. Various analytical models, such as the Taur model and Fasarakis model have been used to analyze the short and long-channel effects of the DG-FINFET. The output characteristics of the transistor are a plot of the variation in drain current (Id) for the varying VDSs for a fixed VGS. Output characteristics curves are obtained for varying VGSs.

The forced stack leakage reduction technique applied to a FinFET inverter circuit is shown in Fig. 1. The waveforms used to analyze the static and short circuit- powers are shown in Fig.2.

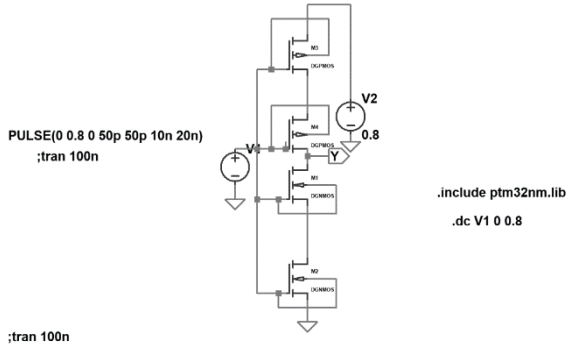

Fig 1. FinFET based forced stack circuit.

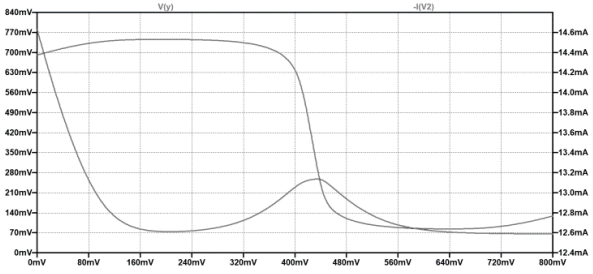

Fig. 2. DC steady state characteristics (red) and short circuit current (blue) in the FinFET based forced stack circuit.

4. System Description and Design

There has been exponential growth in energy efficiency strategies based on daylight and artificial light. An intelligent lighting control system helps maintain the desired illuminance level in an office room by wirelessly controlling LED luminaires and window blinds [34]. Various low-power sensors installed at different nodes collect data from the environment. As mesh networks are self-healing and can communicate with multiple nodes, a DigiMesh network was constructed using the XBee module to determine the connectivity between modules locally. LED luminaires are controlled by the NXP JN516x controller, which determines the required dimming levels based on occupancy and daylight availability. Inputs taken from the photosensor, occupancy sensor, and temperature sensor are fed into an ANFIS-based controller that predicts the Venetian blind position and the dimming levels for the luminaires [35, 36].

The controller for the luminaires and the motor blinds are powered through the indoor solar panel. The boost converter in the system is designed using the MOS transistor and FinFET transistor in this work. The irradiance is estimated based on the total solar irradiance and building information modelling. It changes with window orientation. The irradiance obtained in the test room is from a spectrally tunable and light-level controllable luminaire. Human-centric lighting is the future lighting requirement of buildings; this has also been considered when designing power management systems.

There is a negative correlation between the subthreshold leakage current and the threshold voltage. Utilizing strategies to reduce this

leaking power component becomes crucial as a result. Leakage power is often divided into 2 categories:

1. Leakage Control in Standby Mode: Techniques such as power gating and a super cut-off CMOS are utilized for spillage reduction. In these techniques in the idle state, the circuit is cut off from the supply voltage rails [37].
2. Leakage Control in Active Mode: Techniques such as forced stacking and sleepy stacking are most used for reducing leakage current in runtime mode [38].

1. Results

The combined illuminance from daylight and artificial light falls on the indoor solar panel [39]. For a given room, at different times of day, the total interior illuminance and external daylight on the window are measured, and the indoor irradiance is calculated from the interior illuminance. The indoor irradiance is calculated from interior illuminance using Eq (6). LTspice is used to simulate the switching regulators, both CMOS-based and FinFET-based circuits; Table 1 shows the MOS transistor and FinFET specifications considered in this work obtained from [40].

$$1000W/m^2 = 120000\ lux \quad (6)$$

Table 1. CMOS and FINFET specifications

Specifications	FinFET	CMOS
Technology (nm)	32	180
Gate Length (nm)	16	40
Oxide thickness (nm)	1.4	4.9
VDD (V)	0.9	1.2
Thickness fin (nm)	80	-
Height fin (nm)	32	-
Threshold Voltage (Vth0)	0.29	0.366

1.1 Measurement of power dissipation components:

The leakage currents and short-circuit currents for the CMOS-based and FinFET-based circuits are obtained from the transfer characteristics and by plotting the current through VDD [41, 42]. Different low-power circuits, such as dual VDD, forced stack, and sleepy transistor circuits are applied to CMOS-based and FinFET-based inverters [43]. Fig. 3 shows a CMOS-based inverter with a forced stack low-power technique used to analyze the static and short-circuit powers. Table 2 compares the leakage power and short-circuit power of CMOS-based and FinFET-based circuits with various low-power techniques, such as forced stacking, sleepy transistors, and dual VDD. FinFET-based sleepy transistors in low-power mode have the least leakage power and lowest short-circuit power. This reduction is obtained due to the independent control of the FinFET gates. Although the shorted gate mode of the FinFET has higher leakage currents, it is fastest under all load conditions.

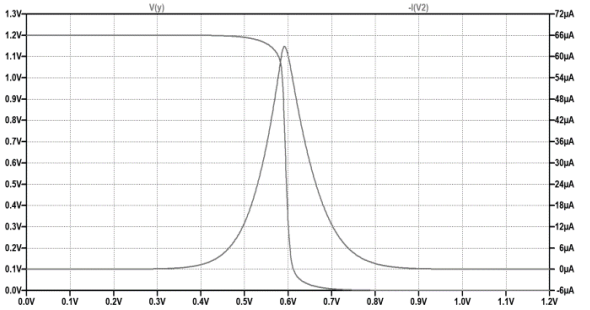

Fig. 3. CMOS-based inverter characteristics with the forced stack low-power technique for analyzing power components.

The combined illuminance obtained from daylight and spectrally tunable and dimmable artificial light falls on the indoor solar panel. For an output of 120 mV from the indoor solar panel, a converter is designed using CMOS and FinFET.

Table 2. Comparison of the power components of FinFET-based and CMOS-based circuits using low-power Techniques.

Circuits	Leakage current	Short circuit
CMOS inverter	9.59 uA	295.07 uA
CMOS – forced stack	612.517 nA	62.8 uA
CMOS -sleepy transistor	1.154 uA	123.32 uA
CMOS – dual VDD	41.25 nA	102.77 uA
FinFET inverter (shorted Gate mode)	490.19 uA	6.054 Ma
FinFET inverter – forced stack (shorted Gate mode)	279.07 uA	2.52 mA
FinFET inverter -sleepy transistor (shorted Gate mode)	1.213 uA	1.67 uA
FinFET inverter – dual VDD (shorted Gate mode)	7.52 uA	3.19 mA

Circuits	Leakage current	Short circuit
FinFET inverter (Low Power Mode)	8.12 uA	626.74uA
FinFET inverter – forced stack (Low Power Mode)	1.11 uA	104.79 uA
FinFET inverter -sleepy transistor (Low Power Mode)	10.19 nA	480 nA
FinFET inverter – dual VDD (Low Power Mode)	2.29 uA	198.89 Ua

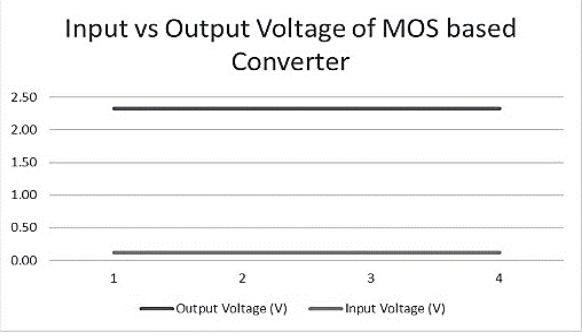

Fig. 4. Input and output voltages of the converter designed using the MOSFET

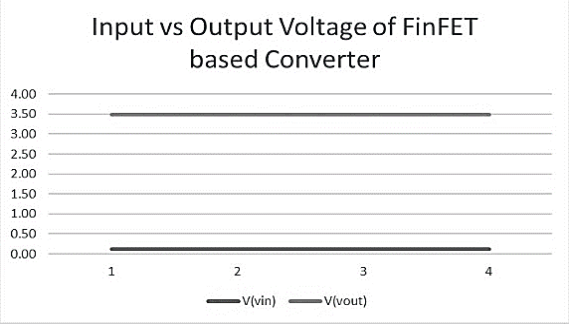

Fig. 5. Input and output voltages of the converter designed using FinFET.

The average power consumed by the FinFET-based power management circuit was 1.1949 mW.

The average power consumed by the CMOS-based power management circuit was 1.3148 mW.

A 9% improvement in average power consumed is observed in the FinFET-based power management circuitry compared with the CMOS-based power management circuitry.

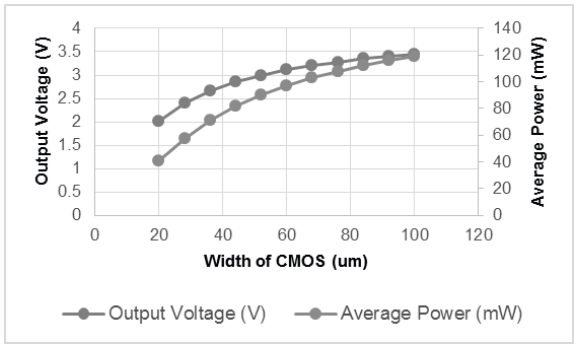

Fig. 6. (a) Variation in the output voltage and average power with respect to the width of the transistor in the CMOS-based power converter.

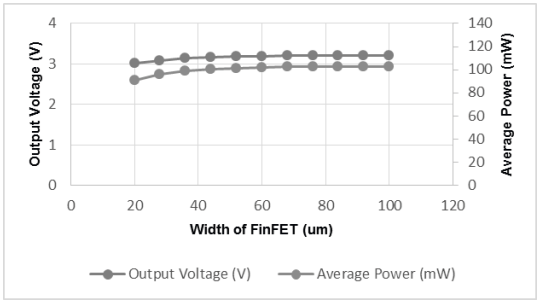

Fig. 6. (b) Variation of output voltage and average power with respect to the width of the transistor in the FinFET-based power converter.

6. Conclusion

The development of low-power Internet of Things devices can be accomplished through indoor solar energy harvesting. The primary driver of the global FinFET market technology is the growing demand for higher device performance and smaller semiconductors. Designing effective DC-DC converters is crucial in energy harvesting systems. The switched-capacitor DC-DC converter has recently attracted much attention. However, the efficiency of the switched-capacitor DC-DC converter is limited because of conduction loss, bottom plate parasitic loss, gate drive loss, and control circuit overhead. Thus, technologies for high-density on-chip capacitors with low bottom plate parasitic potential and the use of FinFET-based designs are required to improve converter efficiency. Additionally, reconfigurable architectures that minimize the voltage swing of bottom plate capacitors and the automatic gain selection and highly efficient regulation techniques need to be explored. Furthermore, the use of other nanoelectronics devices, such as Carbon

Nanotubes (CNFET) and Gallium Nitride (GaN) to design low-power management circuits can be explored. This work can be extended to predict leakage power based on circuit parameters such as doping, oxide thickness, the W/L ratio, technology nodes, and threshold voltage. Additionally, the dynamic and leakage power consumption may be optimized for a given technology node and application.

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